REMARKS

Applicant respectfully requests reconsideration and allowance in view of the following remarks. Applicants incorporate prior arguments made in response to previously issued Office Actions.

Rejections Under 35 U.S.C. § 112

In the Office Action, claims 1-5 stand rejected under 35 U.S.C. § 112. The Office Action inexplicably asserts a belief that Applicant admits "that a hardware processor is in fact necessary" (page 2, lines 7-9). Applicant has made no such admission. Applicant respectfully submits that the grounds for rejection provided in the Office Action are unsubstantiated and the resulting rejections are improper.

In Applicant's response of 05/04/2005, Applicant challenged the Office Action's characterization of direct memory access ("DMA") noting that at least some traditional DMA controllers require programming (*see* prior response at page 2, lines 13-26) whereas the Examiner contended that DMA required no processor involvement. Applicant concluded that a processor would be required to execute at least some software to configure a programmable DMA controller. An example may be enlightening: in the ubiquitous Windows Operating System (Windows Software), a CPU (processor) may use a hardware DMA controller for direct memory access to various plug and play devices. Some plug and play devices may support DMA while other plug and play devices may not support DMA. Upon insertion of a plug and play device, it will be appreciated by one of reasonable skill in the art that Windows software must determine the capabilities of the plug and play device and configure the DMA controller to enable, disable and configure DMA function accordingly. In this example, a hardware DMA approach is taken but the use of the CPU (processor) is necessary to execute a portion of the Windows software used for configuration of DMA. Therefore, the processor is needed for DMA and the Office Action's interpretation of direct memory access as precluding processor involvement excludes commonly used hardware DMA systems and consequently must be flawed.

Nevertheless, even if it is assumed *arguendo* that direct memory transfer by definition requires that the processor is not used, the analysis of the claims of the present Application is defective. Independent claim 1 recites first and second processors and a DMA engine adapted to

be executed *by a processor of the first and second processors*. One of reasonable skill in the art will easily appreciate that the invention claimed in claim 1 includes direct memory access regardless of interpretation of the term "DMA," since one of the two recited processors need not be involved in direct memory transfer operations. Specifically, if the first processor executes the DMA engine, the second processor can execute an instruction that causes a DMA transfer to be initiated without involvement of the second processor. Therefore, the claims of the present application can not be said to redefine the term "direct memory access," and even under the flawed interpretation adopted in the Office Action, the claims particularly point out and distinctly claim the subject matter of the present invention.

Having demonstrated that the usage of direct memory access in the claims cannot reasonably be said to be abnormal, Applicant submits that usage of the word "software" to qualify the term "DMA" will be readily appreciated by one of reasonable skill in the art to mean DMA implemented in software.

For at least these reasons, Applicant respectfully submits that the rejection of Claims 1-5 under § 112 is improper and should be withdrawn.

Rejections Under 35 U.S.C. § 103

In the Office Action Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,884,027 to Garbus et al. ("Garbus") in view of "Structured Computer Organization" by Tanenbaum.

Tanenbaum is offered in the Office Action merely in support of the aphorism that "hardware and software are logically interchangeable" (page 5, lines 3-4). While Applicant submits that one of reasonable skill in the art will appreciate that the Tanenbaum aphorism does mean that all hardware is replaceable by software, it is of greater significance that Tanenbaum cannot does not teach any other substantive limitations of the claims. Therefore, Applicant submits that the § 103 rejections in the Office Action have been shown to be improper because Garbus does not teach, suggest or otherwise render obvious all of the limitations of the claims.

It is respectfully submitted that the Examiner has not met his burden of factually supporting any *prima facie* conclusion of obviousness. MPEP § 2142 provides that to establish a *prima facie* case of obviousness:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

> art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Garbus does not teach or suggest all of the claim limitations. For example, Claim 1 requires an instruction memory coupled to first bus and second bus, having a software DMA stored therein. Garbus does not have such instruction memory. Importantly, the Office Action does not address the absence of such an instruction memory in Grabus and acknowledges that Garbus does not teach a software DMA engine as required by claim 1.

In making its case for obviousness, the Office Action presents as evidence a conclusory statement that it would have been obvious to implement various Garbus hardware elements in software. Applicant disagrees. The Examiner's resistance to a definition of direct memory access as being other a system independent of a processor (*see* Office Action at page 4 lines 1-2) and the teachings of Tanenbaum evidence the non-obviousness of the software DMA engine set forth in the claims. For example, Tanenbaum states that:

> As time progressed, it became obvious to hardware designers that certain operations were being performed frequently enough to justify constructing special hardware circuits to execute them directly (to make them faster). The result was a trend toward moving operations downward to a lower level. (page 11, third paragraph).

Tanenbaum continues by stating that a reverse trend became apparent and concludes that programmers need not be aware of the messy details of the underlying levels (page 11, fourth paragraph and page 12, final paragraph). It is submitted that a fair reading of Tanenbaum would suggest that it would have been obvious to implement the repetitive moving of data of DMA in hardware to improve speed. Thus, Tanenbaum should be read as teaching away from the present invention.

Further, in discussing movement from hardware to software, Tanenbaum refers to migration from hardware to microcode. It will be appreciated by one of ordinary skill in the art that a microcode version of a DMA controller and software DMA engine loadable by a processor from instruction memory are distinctly different implementations.

Additionally, the Office Action proves no motivation for moving DMA from hardware or microcode to software. Although a superficial reading of Tanenbaum may be interpreted as suggesting that the division of hardware and software is arbitrary, Applicant submits that it is

understood in the prior art that DMA is implemented in hardware or microcode to reduce processing overhead. This latter view is echoed in the Office Action at page 4, lines 1-2 and for the Office Action to state otherwise creates an internal inconsistency.

Nor can Tanenbaum alone be alleged to provide motivation to combine Garbus and Tanenbaum. Such allegation would rely on circular logic motivated by improper use of hindsight. Therefore, Applicant submits that the § 103 rejections of claims 1-5 are improper and should be withdrawn.

Regarding claims 6-9, it is noted that claim limitation requires a computer system as described in the claim as having two or more processors having a memory coupled to each of the two or more processors. Applicants submit that claims 6-9 are also improperly rejected for the reasons discussed above.

In summary, for at least the reasons presented above, Garbus combined with Tanenbaum does not teach or suggest a software Direct Memory Access software in a system comprising two or more processors as claimed in the present application. Accordingly, Applicant respectfully submits that claims 1-9 are allowable over the art of record.

CONCLUSION

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition of allowance and a Notice to that effect is earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975.

Date: September 12, 2005

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: MAIL STOP AF, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on September 12, 2005, by Sachiko Snedden.